CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate (2, 4) of first conductivity type having opposed first (8) and second major surfaces;

a semiconductor component (80) defined adjacent to the first major surface;

a trench (30) extending from the first major surface into the semiconductor substrate, having an inner side (34) facing the semiconductor component and an outer side (36) opposed to the semiconductor component;

a thermal oxide (32) filling the trench (30); and

a channel stop diffusion (18) of second conductivity type extending from the first major surface (8) on the outer side (36) of the trench (30) and further extending under the trench from the outer side (36) to the inner side (34) of the trench.

2. A semiconductor device according to claim 1 further comprising a well (6) of a second conductivity type opposite to the first conductivity type implanted into the first major surface (8) of the semiconductor substrate (2, 4); wherein the trench (30) extends from the first major surface (8) through the well (6) into the substrate (2, 4).

3. A semiconductor device according to claim 2 wherein the semiconductor component (80) is a first transistor, the semiconductor device further comprising:

a second transistor (80) adjacent to the first transistor;

a second trench (30) around the second transistor extending from the first major surface (8) into the semiconductor substrate (2, 4), having an inner side facing the second transistor and an outer side opposed to the second transistor (80); and

a thermal oxide (32) filling the second trench (30);

wherein the channel stop diffusion (18) extends from the first major surface (8) between the first and second trenches under each of the first and second trenches.

4. A semiconductor device according to any preceding claim wherein the semiconductor component (80) is an insulated gate field effect transistor having longitudinally spaced source (20) and drain (22) implants in the well defining a channel region (10) at the first major surface (8) between the source (20) and drain (22) implants.

5. A semiconductor device according to claim 4 comprising a gate oxide (12) over the channel region (10) of the first major surface and a gate (16) over the gate oxide, wherein the gate oxide (12) and gate (16) span the channel region (10) from the trench (30) on one side of the channel region (10) to the trench (30) on the other side of the channel region (10) so that the channel region (10) extends laterally between the trenches (30).

6. A method of manufacturing a semiconductor device including:

providing a substrate (2, 4) of a first conductivity type extending between first (8) and second major surfaces;

forming a trench (30) around a component region (10), the trench extending from the first major surface past the component region into the substrate;

forming thermal oxide (32) filling the trench;

implanting a dopant (64) of the second conductivity type along the trench (30) and offset outwards from the centre of the trench (30) away from the component region (10); and

diffusing the dopant (64) so that it extends underneath the trench (30).

7. A method according to claim 6 further comprising the step of implanting a well (6) of a second conductivity type opposite to the first conductivity type at the first major surface (8);

wherein the component region (10) is formed in the well (6) and the trench (30) extends from the first major surface (8) through the well (6) to the substrate (2, 4).

8. A method according to claim 6 or 7 wherein the step of implanting a dopant of second conductivity type is carried out by forming a mask (60) having an opening (62) above the trench (30), the opening being offset away from the component region (10), and then implanting the channel stop dopant (64) through the mask.

9. A method according to claim 6, 7 or 8 wherein the mask (60) is patterned to form the opening using a reduction stepper.

10. A method according to any of claims 6 to 9 further comprising the steps of:

forming longitudinally spaced source (20) and drain (22) diffusions defining a channel region (10) therebetween in the component region;

depositing a gate oxide (12) layer at least over the channel region (10);

depositing a gate (16) over the gate oxide layer (12), the gate extending laterally across the channel region (10), having the trench (30) at each end of the gate.